PWM Switched Capacitor Converter with Switched-Capacitor-Inductor Cell for Adjustable High Step-Down Voltage Conversion

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***Abstract*— High step-down voltage conversion is necessary to bridge the voltage gap between main power converters and low-voltage auxiliary electronics in power conversion systems. Switched capacitor converters (SCCs) are an attractive candidate as a high step-down converter, but their poor voltage regulation capability may limit their applications. PWM SCCs with adjustable high step-down voltage conversion are proposed in this paper. The proposed PWM SCCs can be derived from traditional SCCs by replacing an energy transfer capacitor with a switched-capacitor-inductor (SCL) cell that comprises inductors, capacitors, and diodes to realize PWM-controllable voltage conversion. The voltage step-down ratio of the proposed PWM SCCs is not only PWM-controllable but also adjustable with structures of SCCs and SCL cells. Two representative PWM SCCs were taken as examples to perform the operational analysis. The prototypes of both representative PWM SCCs were built and tested to demonstrate the proposed concept.**

***Index Terms* — High step-down voltage conversion, PWM cell, switched capacitor converter**

I. Introduction

In power conversion electronics systems, efficient main converters determine systems' performance and are functionally at the center of the systems. Meanwhile, ancillary and auxiliary electronics, including control circuits, measurement systems, and digital signal processors, etc., also play important roles and are crucial for power conversion systems. In general, main converters, particularly for high-power applications, operate at a relatively high voltage level, whereas ancillary and auxiliary electronics require a low dc voltage supply, meaning a high step-down voltage conversion is necessary to bridge the voltage gap between main and auxiliary systems.

PWM buck converters are widely used for nonisolated step-down voltage conversion. The voltage conversion ratio of PWM buck converters is simply proportional to the duty cycle, and hence the duty cycle tends to be extremely low for applications requiring high step-down voltage conversion. The extreme duty cycle operation is well known to trigger serious issues, such as impaired output voltage regulation and decreased power conversion efficiency due to increased switching and conduction losses [1].

The simplest approach to preclude the extreme duty cycle operation issues is to use cascaded buck converters. However, efficiency penalty due to multiple power conversion stages is an inevitable disadvantage. With an isolated forward or flyback converter, high step-down voltage conversion can be easily achieved by properly determining a transformer's turn ratio. For nonisolated applications, tapped-inductor (TI)-based PWM buck converters [1] would be a powerful solution. All these approaches, however, have the common issue that switches have to be rated for exceeding the full input voltage, posing issues originating from high voltage ratings, such as increased on-resistance and slower switching characteristics. As for TI-based converters, even higher voltage rating switches are necessary because of a TI's leakage inductance which naturally causes a voltage spike. Although some other nonisolated high step-down converters have been proposed [2], [3], the issue of high voltage rating switches firmly remains.

In input-series–output-parallel (ISOP) converters [4], a high input voltage is divided by series-connected converters, allowing the voltage rating for switches to be mitigated and the use of MOSFETs, even for high-voltage applications. Rainstick converters, which are basically multi-stacked buck-boost converters dividing a high input voltage, have also been

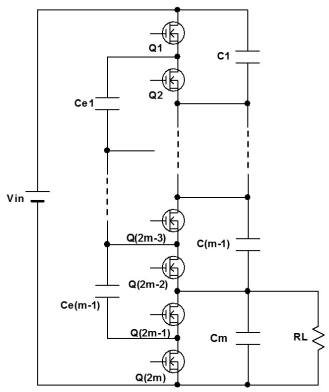

Fig. 1. Generalized ladder-type switched capacitor converter (SCC) comprising *m* static capacitors connected in series.

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proposed [5]. However, the magnetic component count (i.e., transformers and inductors for ISOP and Rainstick converters, respectively) is proportional to the number of series-connected converters, increasing the system volume and cost. Meanwhile, various kinds of high step-down interleaved buck converters have been developed [6]–[9]. Switches' voltage ratings can be reduced, but multiple carrier waves are necessary, increasing the complexity of control circuits.

Switched capacitor converters (SCCs) consisting of switches and capacitors can achieve high step-down voltage conversion, and their voltage conversion ratios are dependent on the number of capacitors used. The larger the number of capacitors used, the higher will be the step-down ratio, immune to the issue of high voltage rating switches [10]–[12]. Although SCCs offer high step-down voltage conversion ratio at high power density, their relatively poor output voltage regulation capability is often cited as a top concern. The output voltage in many ordinary topologies can only be regulated for a narrow range by means of PWM or PFM controls [13], [14] that virtually adjust the equivalent resistance of SCCs. However, their power conversion efficiencies are unavoidably lowered because it is essentially a dissipative voltage regulation method. In other words, ordinary SCCs achieve high power conversion efficiency only at a fixed conversion ratio [15]–[17], and their efficiencies quickly decrease as the conversion ratio moves away from the fixed value.

Two-stage power conversion architectures using an unregulated SCC and PWM buck converter for first- and second-stage converters, respectively, have been proposed to cope with the duty cycle limitation issues [18]–[22]. The first-stage SCC operates as a high power density voltage divider, while the second-stage PWM buck converter regulates the load voltage. Although the two-stage architectures offer controllable high step-down voltage conversion immune to the switch voltage rating issue, an increased system cost is likely because of the additional first-stage SCC.

With additional magnetic components or utilizing parasitic inductances, the issue of the poor voltage regulation capability of SCCs can be addressed by realizing resonant or phase-shift operations [23]–[27]. Resonant SCC comprising a typical SCC with an added resonant inductor can regulate the load voltage while reducing switching losses and EMI [23]–[26]. Phase-shift SCCs have also been proposed to improve the voltage regulation capability [27]. However, to achieve high step-down voltage conversion, the required numbers of capacitors and resonant inductors tend to soar, increasing the volume and cost of the converter. Meanwhile, various kinds of single-inductor PWM SCCs have also been proposed to realize good voltage regulation [28]–[31], but numerous switches and capacitors are still necessary for applications needing high step-down conversion ratios.

Multi-level SCCs realize PWM-controllable voltage conversion with a single inductor [32]–[34]. In addition to the PWM-controllability, the voltage conversion ratio can be arbitrarily extended by increasing the number of flying capacitors. However, (n−1) carrier waves are necessary to generate multiple PWM signals for an n-level converter, resulting in complex and costly control, especially for high step-down applications.

In this paper, PWM SCCs with adjustable high step-down voltage conversion ratios are proposed. The proposed PWM SCCs can be derived based on a traditional SCC by replacing an energy transfer capacitor with a switched-capacitor-inductor (SCL) cell comprising capacitors, inductors, and diodes. SCL cells realize PWM-controllability. The voltage conversion ratio of the proposed PWM SCCs depends on the structures of both the SCC and SCL cell, allowing two design freedoms (i.e., SCC and SCL cell structures) to be flexibly used to determine the step-down ratio according to applications and requirement. The rest of this paper is organized as follows. Section II reviews traditional ladder-type SCCs and proposes SCL cells, while two representative PWM SCCs are derived by combining the SCCs and SCL cells. In Section III, the voltage step-down ratios of the derived PWM SCCs are mathematically yielded and compared with that of a traditional PWM buck converter. Detailed operational analyses are performed in Section IV. In Section V, prototypes of both representative topologies are built and tested, and detailed loss analyses are performed based on the operational analysis performed in Section IV. The proposed PWM SCCs are compared with conventional ones from various aspects in Section VI. Section VII introduces extended topologies of the proposed PWM SCCs.

II. PWM Switched Capacitor Converter

A. Traditional Ladder-Type Switched Capacitor Converters

The generalized form of traditional ladder-type SCCs is shown in Fig. 1. Odd- and even-numbered switches are alternately driven with a fixed duty cycle of 50%, and all capacitor voltages automatically become nearly uniform. C_1–C_m are static capacitors that divide the input voltage into m levels while C_{e1}–$C_{e(m-1)}$ are energy transfer capacitors that deliver charges between adjacent static capacitors. As m

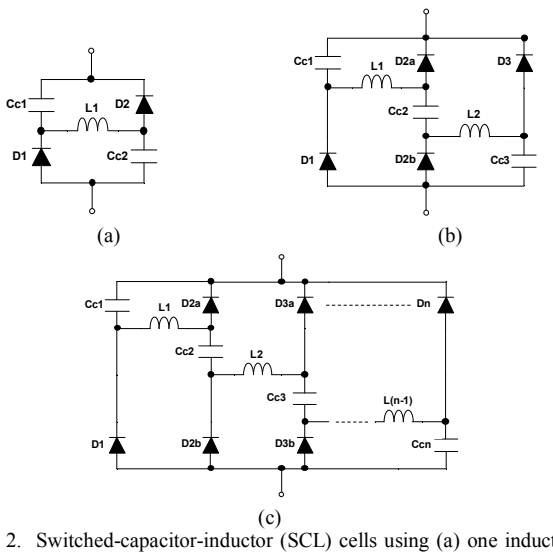

Fig. 2. Switched-capacitor-inductor (SCL) cells using (a) one inductor and two capacitors (1L-2C), (b) two inductors and three capacitors (2L-3C), and (c) n inductors and (n + 1) capacitors.

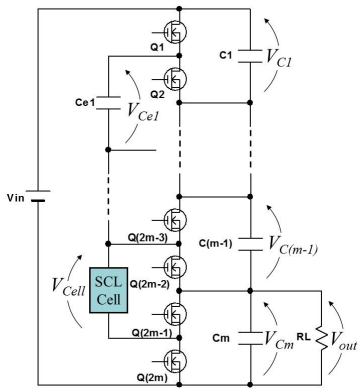

Fig. 3. Generalized PWM SCC comprising m static capacitors connected in series.

capacitors (C_1–C_m) connected in series and one capacitor (C_m) are connected to the input V_{in} and output load R_L, respectively, the voltage step-down ratio is $1/m$, and hence the step-down ratio depends on the number of static capacitors connected in series. The larger the number of static capacitors connected in series, the greater will be the step-down ratio. Traditional ladder-type SCCs, however, should be used so that the step-down ratio is fixed. Otherwise their power conversion efficiencies quickly drop, as mentioned in Section I, likely limiting applications. In the following sections, SCCs comprising two and three static capacitors connected in series are taken as examples and are called as 2s- and 3s-SCCs, respectively, for the sake of convenience.

B. Switched-Capacitor-Inductor (SCL) Cell

Proposed PWM SCCs can be derived by replacing an energy transfer capacitor with a switched-capacitor-inductor (SCL) cell. Representative circuits as well as a generalized structure of SCL cells are shown in Fig. 2. The SCL cells consist of n inductors, n+1 capacitors, and 2n diodes (where n is an arbitrary integer larger than 1). For convenience, the circuit comprising one inductor and two capacitors is called as 1L-2C SCL cell, while that comprising two inductors and three capacitors is called 2L-3C SCL cell.

The SCL cells operate as an energy transfer capacitor in a traditional SCC, but their terminal voltages during charging and discharging periods differ, as will be discussed in Section III-A. The larger the value of n, the greater will be the difference between charging and discharging terminal voltages, resulting in a greater voltage step-down ratio. A detailed operational analysis will be performed in the next section.

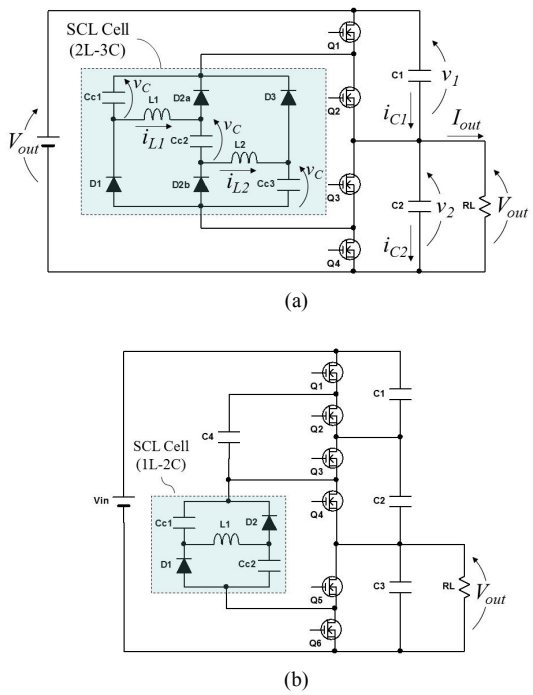

Fig. 4. Proposed high step-down PWM SCCs based on (a) 2s-SCC with 2L-3C SCL cell and (b) 3s-SCC with 1L-2C SCL cell.

C. PWM Switched Capacitor Converters

By replacing an energy transfer capacitor in a traditional SCC with an SCL cell shown in Fig. 2, the proposed high step-down PWM SCCs can be derived. The generalized PWM SCC is shown in Fig. 3; the energy transfer capacitor $C_{e(m-1)}$ shown in Fig. 1 is replaced with the SCL cell. Static capacitors of C_1–$C_{(m-1)}$ and energy transfer capacitors of C_{e1}–$C_{e(m-2)}$ are identical to those in the traditional SCC, meaning that their voltages are automatically unified. Meanwhile, the voltage of C_m, V_{Cm}, is lower than the others thanks to the operation of the SCL cell, as will be explained in detail in the next section.

Representative topologies based on 2s- and 3s-SCCs with 2L-3C and 1L-2C SCL cells, respectively, are also shown in Fig. 4. These circuits correspond to m = 2 and n = 2, and m = 3 and n = 1. In the following sections, the PWM SCCs shown in Fig. 4 are analyzed and tested as representative topologies. Similar to conventional SCCs, even- and odd-numbered switches in the proposed PWM SCCs operate in a complementary mode. Hence, compared with multi-level SCCs requiring multiple carrier waves, the control circuit of the proposed PWM SCCs

TABLE I
ENERGY DENSITY COMPARISON BETWEEN CAPACITORS AND INDUCTORS

	Part Number	Manufacturer	Value	Rating	Dimension [mm]	Energy Density [μJ/mm^3]
Inductor	7447709330	Wurth Electronics	33 μH	4.2 A	12×12×10	0.202
	7447709150	Wurth Electronics	15 μH	6.5 A	12×12×10	0.22
Al Electrolytic Capacitor	UUD1A331MNL1GS	Nichicon	330 μF	10 V	8×8×10	25.8
	PCE3909TR-ND	Panasonic	470 μF	25 V	10×10×10	147
Tantalum Capacitor	TPSE337M010R0100	AVX	330 μF	10 V	7.3×4.3×4.3	122
	T491X107K025ZT	Kemet	100 μF	25 V	7.3×4.3×4.3	232
Ceramic Capacitor	GRM32ER61A107ME20L	Murata	100 μF	10 V	3.2×2.5×2.7	231
	C7563X7R1E476M230LE	TDK	47 μF	25 V	7.5×6.3×2.6	120

can be simplified.

Despite at least one inductor necessary for the PWM-controllability, the superior energy density of capacitors would allow the proposed PWM SCC to achieve higher power density than traditional inductor-based converters. Energy densities of aluminum electrolytic, tantalum, and multi-layer ceramic capacitors (MLCCs) are compared with those of similarly scaled inductors, as shown in Table I. The energy density of discrete capacitors is generally within a range of more than three orders of magnitude over that of inductors, driving expectations of the superior power density of SCC-based converters. Previous works reported SCC-based converters realize reduced circuit volume or higher power density compared to traditional inductor-based converters [34], [35].

III. Step-Down Voltage Conversion Ratio of PWM SCCs

A. Operation of SCL Cell

As briefly mentioned in Section II-B, the SCL cells operate as energy transfer capacitors. The current flow directions of the generalized SCL cell [see Fig. 2(c)] during charging and discharging periods are shown in Figs. 4(a) and (b), respectively. All the energy storage elements (inductors and capacitors) are charged in series during the charging period. During the discharging period, on the other hand, all of them discharge in parallel through respective diodes.

For the sake of simplicity, it is assumed that all circuit elements are ideal with no ESR, all inductors have the same inductance, and all diodes are ideal with no forward voltage drop. As all inductors and capacitors discharge in parallel during the discharging period [see Fig. 5(b)], capacitor voltages V_{Cc} and the voltage applied across each inductor $V_{L\text{-}B}$ are expressed as

$$V_{Cell-B} = V_{Cc} = V_{L-B}, \tag{1}$$

where $V_{Cell\text{-}B}$ is the terminal voltage of the SCL cell during the discharging period, as designated in Fig. 5(b). During the charging period, on the other hand, all inductors and capacitors are charged in series, and hence, the terminal voltage $V_{Cell\text{-}A}$ is

$$V_{Cell-A} = nV_{L-A} + (n+1)V_{Cc}, \tag{2}$$

where $V_{L\text{-}A}$ is the inductor voltage during the charging period. From the volt-second balance on inductors, the voltage relationship between $V_{Cell\text{-}A}$ and $V_{Cell\text{-}B}$ can be yielded as

$$\frac{V_{Cell-B}}{V_{Cell-A}} = \frac{d}{d+n}. \tag{3}$$

where d is the duty cycle of the charging period. The ratio of $V_{Cell\text{-}B}$ to $V_{Cell\text{-}A}$ depends on d, realizing PWM-controllability. Furthermore, this ratio can be adjusted with n, which is the arbitrary integer that represents the structure of SCL cells.

To provide an operational example in a practical topology, the current flow directions of the PWM SCC shown in Fig. 4(a) are illustrated in Fig. 6. The PWM SCC operates in two modes of Modes A and B, which respectively correspond to the charging and discharging periods for the SCL cell. In Mode A, the odd-numbered switches are on, and the inductors and capacitors in the SCL cell are charged. In Mode B, the SCL cell is connected to C_2, and all inductors and capacitors in the PWM cell discharge in parallel.

B. Voltage Step-Down Ratio of PWM SCC

In this subsection, the voltage step-down ratio of the generalized PWM SCC shown in Fig. 3 is derived based on the premise that all circuit elements are ideal with no ESR and no forward voltage drop for diodes. The precise output voltage can be yielded from the state-space modeling, as will be indicated by (30) in Section IV-E. The series connection of C_1–C_m is tied to the input voltage source, while C_m is connected to the load. Voltages of C_1–$C_{(m-1)}$, V_{C1}–$V_{C(m-1)}$, are uniform as V_C, and the input and output voltages, V_{in} and V_{out}, can be expressed as

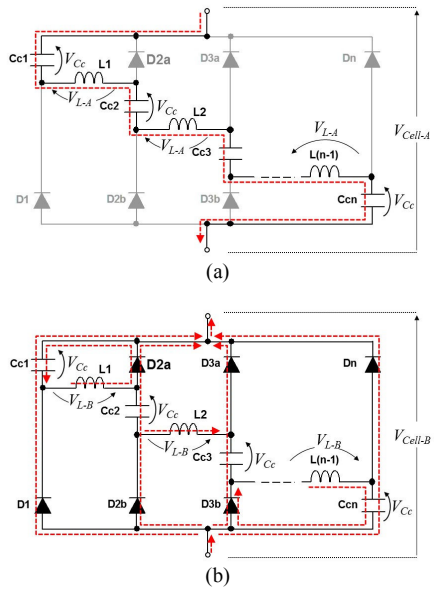

Fig. 5. Current flow directions of SCL cell during (a) charging and (b) discharging periods.

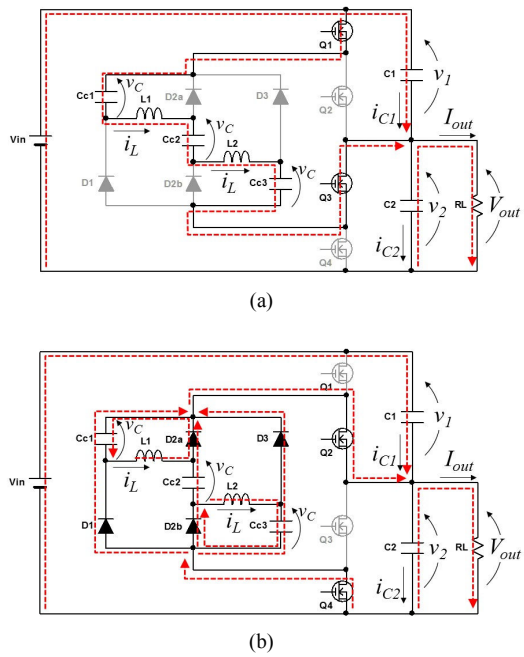

Fig. 6. Current flow directions of 2s-SCC with 2L-3C SCL cell during (a) Mode A and (b) Mode B.

$$\begin{cases} V_{in} = \sum_{i=1}^{m-1} V_{Ci} + V_{Cm} = (m-1)V_C + V_{Cm} \\ V_{out} = V_{Cm} \end{cases}, \quad (4)$$

where i is the subscript number of static capacitors.

Similar to Fig. 6, the SCL cell is connected to $C_{(m-1)}$ and C_m through the odd- and even-numbered switches during Modes A and B, respectively, and hence,

$$\begin{cases} V_{Cell-A} = V_{C(m-1)} = V_C \\ V_{Cell-B} = V_{Cm} \end{cases}. \quad (5)$$

From (3)–(5), the voltage step-down ratio can be generalized as

$$\frac{V_{out}}{V_{in}} = \frac{d}{md + (m-1)n}, \quad (6)$$

where d is the duty cycle of the high-side switches or odd-numbered switches in the proposed PWM SCCs shown in Figs. 3 and 4.

Since the 2s-SCC with 2L-3C SCL cell corresponds to $m = 2$ and $n = 2$, its step-down ratio is yielded as

$$\frac{V_{out}}{V_{in}} = \frac{d}{2+2d}. \quad (7)$$

Similarly, the step-down ratio of the 3s-SCC with 1L-2C SCL cell ($m = 3$ and $n = 1$) is

$$\frac{V_{out}}{V_{in}} = \frac{d}{2+3d}. \quad (8)$$

The step-down ratios of the proposed PWM SCCs as a function of d are compared with that of a traditional PWM buck converter, as shown in Fig. 7. At a given d, the proposed PWM SCCs achieve a greater step-down ratio than does the traditional buck converter, meaning the duty cycle limitation issue can be mitigated.

C. Major Features

Similar to conventional SCCs shown in Fig. 1, the voltage conversion ratio of the proposed PWM SCCs can be adjusted with the number of static capacitors (i.e., m) connected in series that divide the input voltage—the larger the value of m, the greater will be the step-down ratio. In addition, the step-down ratio is also dependent on n. Thus, the voltage step-down ratio of the proposed PWM SCCs is PWM-controllable and adjustable with structures of both SCCs and SCL cells. In other words, two design freedoms—structures of the SCC and SCL cell—can be used to determine the step-down ratio, meaning proposed PWM SCCs can be flexibly designed according to applications and requirements.

The prominent feature of the proposed PWM SCCs is the high step-down voltage conversion capability with fewer switches in comparison with previously reported SCCs. In other words, with a given number of switches, the proposed PWM SCCs achieve greater step-down ratio than do conventional ones. The detailed comparison will be presented in Section VI.

The step-down ratios of the two PWM SCCs (see Fig. 4) are somewhat similar, although their topologies differ. The PWM SCC shown in Fig. 4(a) uses fewer switches, and therefore, driver circuits for MOSFETs can be simpler than those for the circuit shown in Fig. 4(b). In contrast, more inductors and diodes in the SCL cell are necessary, likely resulting in increased circuit volume and less efficient power conversion.

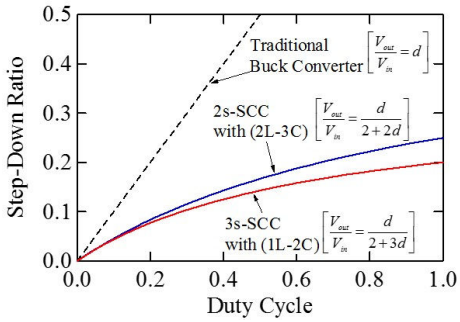

Fig. 7. Comparison between proposed PWM SCCs and traditional PWM buck converter in terms of voltage step-down ratio.

Meanwhile, the topology shown in Fig. 4(b) needs more switches, but reduced numbers of inductors and diodes are advantageous, meaning a proper topology should be chosen considering applications and requirements.

Although only two representative topologies are discussed in this paper, an even greater step-down ratio can be achieved by stacking more static capacitors in SCCs and/or adding more components in SCL cells (i.e., increasing the values of m and/or n). However, for low-voltage applications, forward voltage drops in diodes in the SCL cells inevitably take a large portion of the output voltage, causing significant conduction losses. By taking that into account, the proposed PWM SCCs are considered best suitable for output voltages exceeding, say, around 5 V or so.

IV. Theoretical Analysis

A. Current Waveforms

An equivalent resistance R_{eq} is often introduced to express a characteristic of an SCC. The value of R_{eq} with a fixed duty cycle of 50% is expressed as [36]

$$R_{eq} = \frac{1}{f_S C} \frac{1 + \exp\left(\frac{0.5T}{\tau}\right)}{1 - \exp\left(\frac{0.5T}{\tau}\right)}, \quad (9)$$

where f_S is the switching frequency, τ is the time constant equal to $C \times R$ where C is the capacitance and R is the total resistance of the current loop, including not only the ESRs of the capacitors but also on-resistances of switches. In general, current waveforms of capacitors in SCCs depend on f_S and corner frequency f_{cnr} that is the inverse of the time constant τ (i.e., $f_{cnr} = 1/\tau$). According to the relationship between f_S and f_{cnr}, two operation regions are defined; the fast-switching limit (FSL) and slow-switching limit (SSL) that are the frequency ranges of $f_S >> f_{cnr}$ and $f_S << f_{cnr}$, respectively [15], [37]. The shape of current waveforms depends significantly on this frequency relationship [38].

The equivalent resistance as a function of frequency is depicted in Fig. 8, in which the typical current waveforms in each region are also illustrated. In the SSL region, the value of R_{eq} increases as f_S decreases, and large rush currents flow, causing significant losses as well as an EMI issue. In FSL region, on the other hand, R_{eq} approaches to R as f_S rises, and the current waveforms are a virtually square wave, mitigating

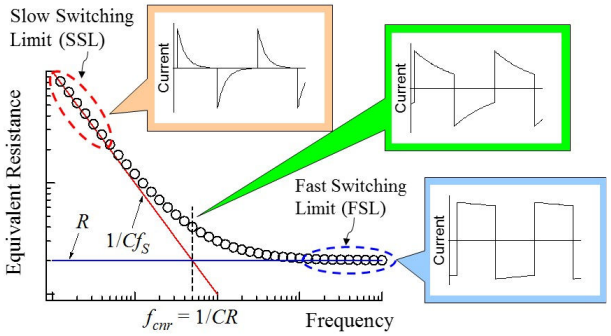

Fig. 8. Equivalent resistance of a capacitor as a function of frequency, and typical current waveforms.

the loss and noise issue.

In general, MLCCs offer superior energy density to other types of capacitors, such as aluminum electrolytic and tantalum capacitors, and their ESR is very low. Because of the low ESR and capacitance, their f_{cnr} tends to exceed those of other capacitors and usually reaches the MHz range. In other words, f_S must be pushed up to the MHz range, otherwise resulting in SSL operations causing significant loss as well as an EMI issue. Operations in the MHz range, however, increases the gate-driving and switching losses, which are proportional to f_S. Furthermore, within such frequency range, equivalent series inductances (ESLs) of components, which have a significant impact on current waveforms, must be taken into account [39]. For MLCCs to be employed while immune to the aforementioned issues, SCCs should operate with a resonant manner, which is outside the scope of this paper.

Aluminum electrolytic and tantalum capacitors, on the other hand, have larger capacitance and ESR, and their f_{cnr} is lower than the MHz range. Values of f_{cnr} of the aluminum electrolytic capacitors used for the prototype of the proposed PWM SCCs, for example, are around 200 kHz if the total resistance R, including ESRs and on-resistances of switches, is factored in (see Section V-A). In other words, FSL operations are feasible with aluminum electrolytic or tantalum capacitors in the range of f_S lower than a few hundred kHz. Thus, in the following sections, operation analyses are performed assuming that PWM SCCs employ aluminum electrolytic capacitors and operate in the FSL region.

B. Charge Vector Analysis

In general, capacitors in an SCC deliver the unique amount of charge depending on their positions, which can be determined based on the charge vector analysis [15], [22]. Here, the flows of charge are focused, and amount of charge delivered is determined based on Kirchhoff's current law (KCL). In this subsection, the charge vector analysis is performed for the PWM SCC shown in Fig. 4(a), as an example.

Charge flow directions in each mode are defined as shown in Fig. 9, in which L_1, L_2, and R_L are depicted as current sources of Q_{L1}, Q_{L2}, and Q_{out}. From KCL at nodes X and Y in Mode A [see Fig. 9(a)], the following set of equations can be obtained;

$$\begin{cases} 0 = q_{in.A} - q_1 - q_{Cc1} \\ 0 = q_1 - q_2 + q_{Cc3} - q_{out.A} \end{cases}. \tag{10}$$

In Mode A, all inductors and capacitors in the SCL cell are charged in series [see nodes a–c in the SCL cell in Fig. 9(a)], and thus,

$$q_{Cc1} = q_{Cc2} = q_{Cc3} = q_{L1.A} = q_{L2.A}. \tag{11}$$

KCL at nodes X' and Y' in Mode B [see Fig. 9(b)] gives

$$\begin{cases} 0 = q_{in.B} + q_1 \\ 0 = -q_1 + q_2 + q_{Cc1} + q_{D2a} + q_{D3} - q_{out.B} \end{cases}. \tag{12}$$

where q_{D2a} and q_{D3} are given by [see nodes a'–c' in the SCL cell in Fig. 9(b)]

$$\begin{cases} q_{D2a} = q_{L1.B} + q_{Cc2} \\ q_{D3} = q_{L2.B} + q_{Cc3} \end{cases}. \tag{13}$$

The charge of inductors as well as Q_{out} is proportional to the mode length, expressed as

$$\begin{cases} (1-d)q_{L1.A} = dq_{L1.B} \\ (1-d)q_{L2.A} = dq_{L2.B} \\ (1-d)q_{out.A} = dq_{out.B} \end{cases}. \tag{14}$$

The voltage variation of the series connection of C_1–C_2 can be presumed as zero because it is connected to the voltage source of V_{in}. Neglecting ESRs of C_1 and C_2, the following equation can be yielded;

$$0 = \frac{q_1}{C_1} + \frac{q_2}{C_2}, \tag{15}$$

where C_1 and C_2 are the capacitance of C_1 and C_2. The charge delivered to the load is assumed to be 1, as

$$1 = q_{out.A} + q_{out.B}. \tag{16}$$

By assuming $q_{Cc1} = q_{Cc2} = q_{Cc3} = q_C$, $q_{L1.A} = q_{L2.A} = q_{L.A}$, and $q_{L1.B} = q_{L2.B} = q_{L.B}$, (10)–(16) can be summarized in the matrix form as

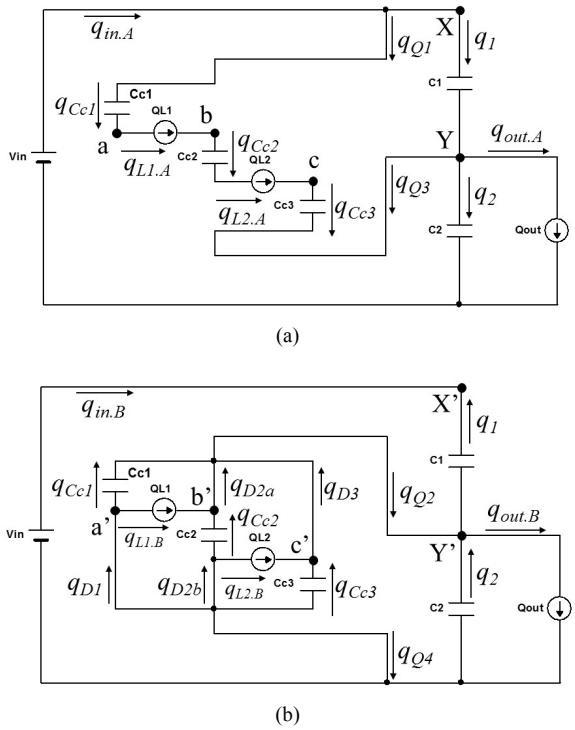

Fig. 9. Charge flow during (a) Mode A and (b) Mode B.

TABLE II
RELATIVE CHARGE FLOWING THROUGH COMPONENTS IN 2S-SCC WITH 2L-3C SCL CELL [SHOWN IN FIG. 4(A)]

Parameter	Charge
q_1	$\frac{C_1}{C_1+C_2}\frac{d(d+1)}{2d+2}$
q_2	$-\frac{C_2}{C_1+C_2}\frac{d(d+1)}{2d+2}$
$q_{Cc1}, q_{Cc2}, q_{Cc3}$	$d/(2d+2)$
$q_{L1\text{-}A}, q_{L2\text{-}A}$	$d/(2d+2)$
$q_{L1\text{-}B}, q_{L2\text{-}B}$	$(1-d)/(2d+2)$
q_{D1}, q_{D2}, q_{D3}	$1/(2d+2)$
q_{Q1}	$d/(2d+2)$
q_{Q2}	$(d+2)/(2d+2)$
q_{Q3}	$-d/(2d+2)$
q_{Q4}	$-(d+2)/(2d+2)$

TABLE III
RELATIVE CHARGE FLOWING THROUGH COMPONENTS IN 3S-SCC WITH 1L-2C SCL CELL [SHOWN IN FIG. 4(B)]

Parameter	Charge
q_1	$\frac{C_1}{C_1C_2+C_2C_3+C_3C_1}\frac{3C_2d^2+(C_2+C_3)d}{3d+2}$
q_2	$\frac{C_2}{C_1C_2+C_2C_3+C_3C_1}\frac{3C_1d^2-C_3d}{3d+2}$
q_3	$-\frac{C_3}{C_1C_2+C_2C_3+C_3C_1}\frac{3(C_1+C_2)d^2+C_2d}{3d+2}$
q_4	$d/(3d+2)$
q_{Cc1}, q_{Cc2}	$2d/(3d+2)$
$q_{L1\text{-}A}$	$2d/(3d+2)$
$q_{L1\text{-}B}$	$2(1-d)/(3d+2)$
q_{D1}, q_{D2}	$2/(3d+2)$
$q_{Q1}-q_{Q3}$	$d/(3d+2)$
q_{Q4}	$(d+2)/(3d+2)$
q_{Q5}	$-2d/(3d+2)$
q_{Q6}	$-2(d+1)/(3d+2)$

$$\begin{bmatrix}0\\0\\0\\0\\0\\0\\0\\0\\1\end{bmatrix}=\begin{bmatrix}-1&0&-1&0&0&1&0&0&0\\1&-1&1&0&0&0&0&-1&0\\1&0&0&0&0&0&1&0&0\\-1&2&3&0&2&0&0&0&-1\\0&0&1&-1&0&0&0&0&0\;0\\C_2&C_1&0&0&0&0&0&0&0\\0&0&0&1-d&-d&0&0&0&0\\0&0&0&0&0&0&0&1-d&-d\\0&0&0&0&0&0&0&1&1\end{bmatrix}\begin{bmatrix}q_1\\q_2\\q_C\\q_{L.A}\\q_{L.B}\\q_{in.A}\\q_{in.B}\\q_{out.A}\\q_{out.B}\end{bmatrix}. \quad (17)$$

From (17), the respective relative charge can be obtained as shown in Table II. Charge flows of switches and diodes, q_{Q1}–q_{Q4} and q_{D1}–q_{D3}, can be yielded from those of capacitors and inductors.

By assuming current waveforms in the PWM SCC are ideal square waves, as mentioned in Section IV-A, the currents flowing through each component in Modes A and B, $I_{k.A}$ and $I_{k.B}$, can be expressed as

$$\begin{cases} I_{k.A}=\frac{q_k I_{out}}{d} & \text{(Mode A)} \\ I_{k.B}=\frac{q_k I_{out}}{1-d} & \text{(Mode B)} \end{cases}, \quad (18)$$

where k is the subscript component symbol and number (i.e., k = C_1…C_2, C_{c1}…C_{c3}, D_1…D_3, Q_1…Q_4, and L_1…L_2). It is noted that either $I_{k.A}$ or $I_{k.B}$ for switches is zero due to their off periods. $I_{k.A}$ for diodes is zero because diodes in the proposed PWM SCC conduct only during Mode B (see Fig. 6).

Although the PWM SCC shown in Fig. 4(a) was analyzed as an example in this subsection, any topologies of PWM SCCs can be analyzed similarly. The results of the charge vector analysis for the PWM SCC shown in Fig. 4(b) are shown in Table III.

C. Simulation Verification for Charge Vector Analysis

Simulation analysis was performed for the 2s-SCC with 2L-3C SCL cell [shown in Fig. 4(a)] at V_{in} = 48 V, V_{out} = 6.0 V, and I_{out} = 6.0 A to verify the charge vector analysis discussed in the previous subsection. The component values used for the simulation were identical to those for the prototype, as will be shown in Table IV. Considering τ of the circuit, f_S was determined to be 200 kHz so that the PWM SCC operates in the FSL region.

The simulation results are shown in Fig. 10. Similar to the waveform shown in the inset of Fig. 8, the waveforms except for the inductor currents were nearly square waves, indicating the FSL operation. As indicated by the minus sign of q_2 in Table II, the polarity of i_{C2} differed from that of i_{C1} and i_{Cc1}–i_{Cc3}. Current values in the simulation analysis matched well with theoretical ones determined from (18) and Table II. The average currents of i_{C1}, i_{C2}, i_{Cc1}, i_{Q2}, and i_{D1} at d = 0.4 in Mode B, for example, were −1.55, 1.02, −1.43, 8.57, and 3.57 A, respectively, while the theoretical values determined from (18) were −1.66, 0.91, −1.43, 8.57, and 3.57 A. Minor mismatches between simulation results and theoretical values are considered due to non-ideal square wave currents as well as neglected ESRs of static capacitors in (15). Despite the minor mismatch, the simulation results implied that the charge vector analysis is a useful method to estimate current

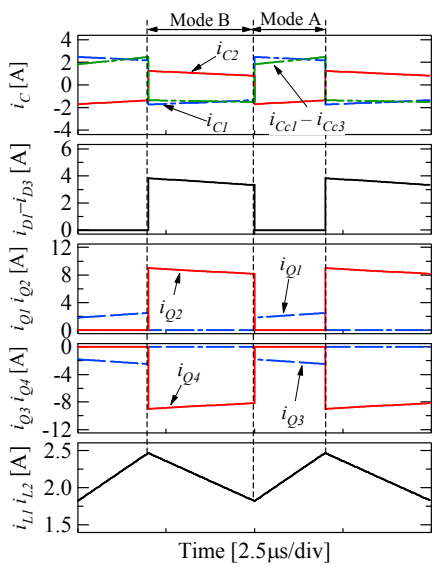

Fig. 10. Simulation waveforms of 2s-SCC with 2L-3C SCL cell.

flowing through respective components in the PWM SCC.

D. Loss Modeling

From the current values determined from (18), Joule loss, diode conduction loss, and switching loss can be modeled. The Joule loss of capacitors, inductors, and switches, $P_{k.Joule}$, is expressed as

$$P_{k.Joule} = \{I_{k.A}^2 d + I_{k.B}^2(1-d)\}r, \tag{19}$$

where r is the resistance of each component. Although this equation can be applied to all components including capacitors, inductors, and switches, the influence of inductors' ripple current is neglected for the sake of simplicity. By taking the ripple current into account, more precise loss modeling for inductors' Joule loss is feasible.

All diodes in the proposed PWM SCCs conduct only during Mode B, which corresponds to 1–d. Hence, the diode conduction loss, $P_{k.Conduction}$, is given by

$$P_{k.Conduction} = V_D I_{k.B}(1-d) \tag{20}$$

The switching loss, $P_{k.Switching}$, can be modeled using the current values determined from (18) and Tables II and III. The minus signs of relative charges flowing through switches, shown in Tables II and III, indicate that current flows from source to drain. In other words, some switches behave as a synchronous switch with no switching loss (i.e., $P_{k.Switching} = 0$). $P_{k.Switching}$ can be approximated based on [40] as

$$P_{k.Switching} = \begin{cases} 0.5V_{DS}(I_{k.A}+I_{k.B})(T_{rise}+T_{fall})f_S & (I_{k.A}, I_{k.B} > 0) \\ 0 & (I_{k.A}, I_{k.B} \le 0) \end{cases}, \tag{21}$$

where V_{DS} is the drain-source voltage, and T_{rise} and T_{fall} are the rise and fall times of switches, respectively. Either $I_{k.A}$ or $I_{k.B}$ of switches is zero during their off periods.

E. State-Space Modeling

State-space modeling for PWM SCCs have been reported [29], and the proposed PWM SCC can be analyzed similarly. In this subsection, the proposed 2s-SCC with the 2L-3C SCL cell shown in Fig. 4(a) is analyzed as a representative. State-space modeling in this subsection is performed on the premise that capacitances of C_{c1}–C_{c3} are uniform as C, inductances of L_1 and L_2 are L, and all capacitors have the same ESR values of r.

The general form of state-space equations is given by

$$\begin{cases} \dfrac{dX}{dt} = AX + BU \\ Y = CX + DU \end{cases}. \tag{22}$$

In the state-space analysis for the proposed PWM SCC shown in Fig. 4(a), the state variables X and input vector U are defined as

$$\begin{cases} X = [i_L \quad v_C \quad v_{C1} \quad v_{C2}]^{T\,T} \\ U = [V_{in} \quad V_D \quad I_{out}]^T \end{cases}. \tag{23}$$

where V_D is the forward voltage drop of diodes, and other variables are designated in Fig. 4(a).

The state-space equation during Mode A is expressed as

$$A = \begin{bmatrix} -\frac{3r}{2L} & -\frac{3r}{2L} & 0 & -\frac{1}{2L} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1 r} & -\frac{1}{C_1 r} \\ \frac{1}{C_2} & 0 & -\frac{1}{C_2 r} & -\frac{1}{C_2 r} \end{bmatrix} \quad B = \begin{bmatrix} \frac{1}{2L} & 0 & 0 \\ 0 & 0 & 0 \\ \frac{1}{C_1 r} & 0 & 0 \\ \frac{1}{C_2 r} & 0 & -\frac{1}{C_2} \end{bmatrix} \tag{24}$$

where r is the ESR of the capacitors. Meanwhile, the state-space equation during Mode B is

$$A = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L} \\ 0 & -\frac{1}{Cr} & 0 & \frac{1}{Cr} \\ 0 & 0 & -\frac{1}{C_1 r} & -\frac{1}{C_1 r} \\ \frac{2}{C_2} & \frac{3}{C_2 r} & -\frac{1}{C_2 r} & -\frac{4}{C_2 r} \end{bmatrix} \quad B = \begin{bmatrix} 0 & -\frac{2}{L} & 0 \\ 0 & \frac{1}{Cr} & 0 \\ \frac{1}{C_1 r} & 0 & 0 \\ \frac{1}{C_2 r} & -\frac{3}{C_2 r} & -\frac{1}{C_2} \end{bmatrix} \tag{25}$$

From (24) and (25), the state-space matrices over a switching cycle can be expressed as

$$A = \begin{bmatrix} -\frac{3r}{2L}d & -\frac{3}{2L}d & 0 & \frac{d-2}{2L} \\ \frac{d}{C} & -\frac{1-d}{Cr} & 0 & \frac{1-d}{Cr} \\ 0 & 0 & -\frac{1}{C_1 r} & -\frac{1}{C_1 r} \\ \frac{2-d}{C_2} & \frac{3(1-d)}{C_2 r} & -\frac{1}{C_2 r} & -\frac{4-3d}{C_2 r} \end{bmatrix} \quad B = \begin{bmatrix} \frac{d}{2L} & -\frac{2(1-d)}{L} & 0 \\ 0 & \frac{1-d}{Cr} & 0 \\ \frac{1}{C_1 r} & 0 & 0 \\ \frac{1}{C_2 r} & -\frac{3(1-d)}{C_2 r} & -\frac{1}{C_2} \end{bmatrix} \tag{26}$$

The output voltage V_{out} is expressed as

$$V_{out} = v_{C2} + i_{C2} r = v_{C2} + (i_{C1} + i_L - I_{out})r. \tag{27}$$

By defining $Y = V_{out}$, we obtain

$$C = \begin{bmatrix} \frac{r}{2} & 0 & -\frac{1}{2} & \frac{1}{2} \end{bmatrix}, \tag{28}$$

$$D = \begin{bmatrix} \frac{1}{2} & 0 & -\frac{1}{2} \end{bmatrix}. \tag{29}$$

V_{out} under steady-state conditions can be yielded by applying $dX/dt = 0$ into (22), as

$$V_{out} = (-CA^{-1}B + D)U. \tag{30}$$

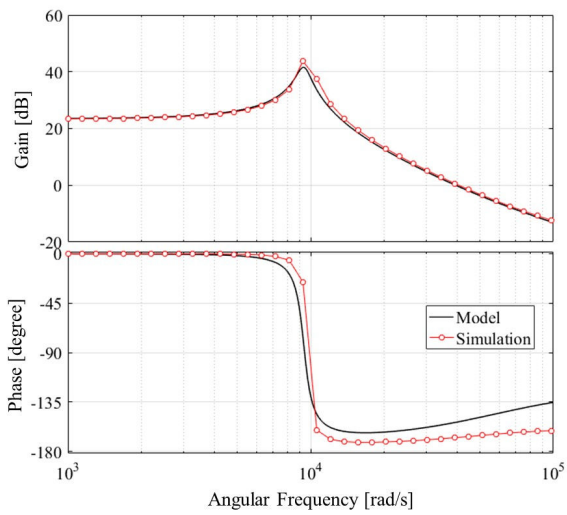

Fig. 11. Bode plots of theoretical model and simulation circuit for 2s-SCC with 2L-3C SCL cell.

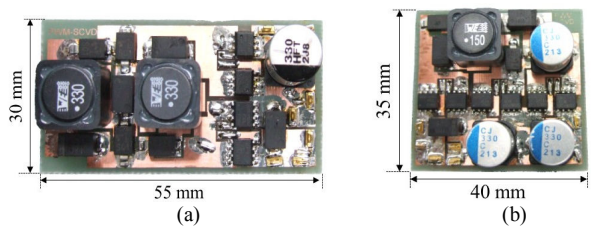

Fig. 12. Photographs of 36-W prototypes of (a) Type 1 (2s-SCC with 2L-3C SCL cell) and (b) Type 2 (3s-SCC with 1L-2C SCL cell).

TABLE IV
COMPONENTS USED FOR PROTOTYPE OF TYPE 1 (2S-SCC WITH 2L-3C SCL CELL)

Component	Value
C_1	Aluminum Electrolytic Capacitor, 330 μF, 12 mΩ
C_2, C_{c1}–C_{c3}	Aluminum Electrolytic Capacitor, 180 μF, 18 mΩ
L_1–L_2	33 μH, 45 mΩ
Q_1, Q_2	N-Ch MOSFET, FDS86240, R_{on} = 35 mΩ
Q_3, Q_4	N-Ch MOSFET, IRF7456, R_{on} = 7 mΩ
D_1–D_3	Schottky Diode, CSL01, V_D = 0.3 V

TABLE V
COMPONENTS USED FOR PROTOTYPE OF TYPE 2 (3S-SCC WITH 1L-2C SCL CELL)

Component	Value
C_1, C_2, C_4	Aluminum Electrolytic Capacitor, 330 μF, 12 mΩ
C_3, C_{c1}–C_{c2}	Aluminum Electrolytic Capacitor, 180 μF, 18 mΩ
L_1	15 μH, 26mΩ
Q_1–Q_4	N-Ch MOSFET, IRF7855, R_{on} = 9 mΩ
Q_5–Q_6	N-Ch MOSFET, IRF7456, R_{on} = 7 mΩ
D_1–D_2	Schottky Diode, CSL01, V_D = 0.3 V

The control-to-output transfer function G is expressed as

$$G = \frac{\Delta Y}{\Delta d} = C(sI - A)^{-1}\left(\frac{\partial A}{\partial d}X + \frac{\partial B}{\partial d}U\right). \tag{31}$$

The Bode plots of the theoretical model (31) and simulation circuit were obtained using MATLAB and PSIM, respectively, and are compared in Fig. 11. Component values of the prototype (see Table IV) were applied with d = 50%, V_{in} = 48 V, I_{out} = 6.0 A, and V_D = 0.3 V. The theoretical model agreed satisfactory with the simulation results, verifying the state-space modeling discussed in this subsection.

V. EXPERIMENTAL RESULTS

A. Prototypes

36-W prototypes of the proposed PWM SCC shown in Figs. 4(a) and (b) were built, as shown in Figs. 12(a) and (b), respectively. For convenience, these prototypes are named as Types 1 and 2, respectively, and the component values are listed in Tables IV and V. The switching frequency f_S was determined to be 200 kHz so that f_S was around the highest value of f_{cnr} in the prototypes—f_{cnr} of the aluminum electrolytic capacitors (180 μF, 18 mΩ) connected through the total resistance of R = 50 mΩ (see Section IV-A) was 1/(90 μF×50 mΩ) = 222 kHz ≈ 200 kHz. Switches were driven by boot-strap synchronous MOSFET drivers (ISL6596), while the driver ICs were powered by static capacitors. In the PWM SCC shown in Fig. 4(a), for example, driver ICs for Q_1–Q_2 and Q_3–Q_4 were powered by C_1 and C_2, respectively, via low-dropout linear regulators. Power conversion efficiencies were measured at V_{in} = 48 V and V_{out} = 5.0 or 6.0 V.

B. Measured and Calculated Efficiencies

Measured power conversion efficiencies and duty cycles of the odd-numbered switches of the prototypes are shown in Fig. 13, and are compared with calculated efficiencies. Losses associated with MOSFET gate drivers were experimentally measured and incorporated into the loss calculation. Both prototypes operated with moderate duty cycles of approximately 0.34–0.40 and 0.42–0.53 at V_{out} = 5.0 and 6.0 V, respectively. Measured and calculated efficiencies matched well in the entire range. The lower efficiencies at V_{out} = 5.0 V were attributed to the diode conduction losses; the forward voltage drops of diodes took a larger portion of the output voltage of 5.0 V than that of 6.0 V.

The measured capacitor voltages and the current waveforms of inductors in Type 1 PWM SCC are shown in Fig. 14, as examples. All the capacitor voltages were virtually constant, although voltage spikes due to parasitic inductances of components and a printed circuit board were observed. The

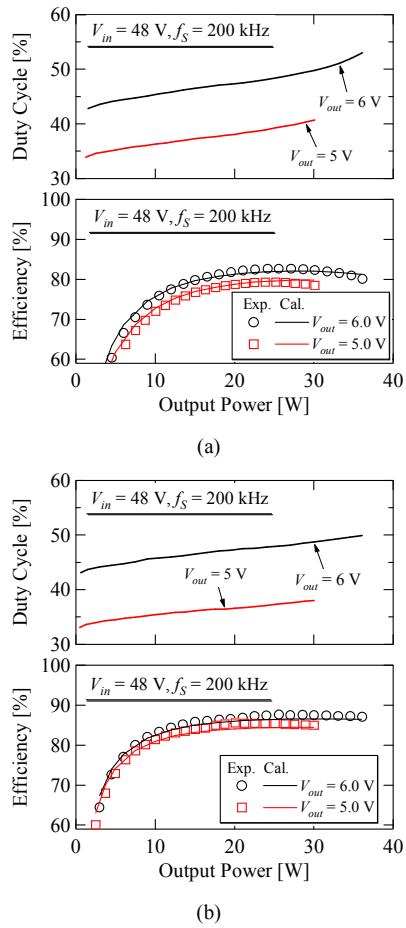

Fig. 13. Measured and calculated efficiencies, and measured duty cycles of (a) Type 1 (2s-SCC with 2L-3C SCL cell) and (b) Type 2 (3s-SCC with 1L-2C SCL cell).

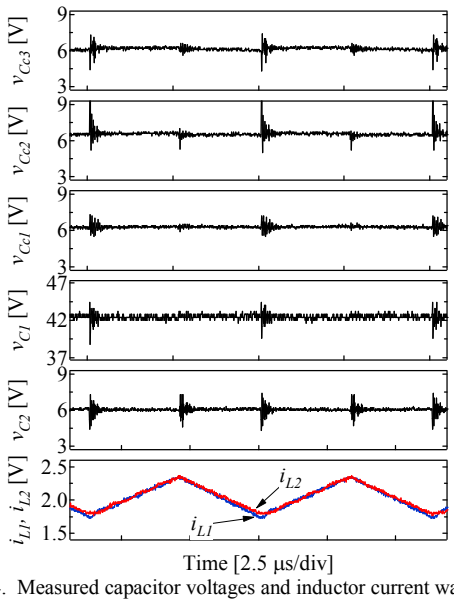

Fig. 14. Measured capacitor voltages and inductor current waveforms of Type 1 (2s-SCC with 2L-3C SCL cell).

slight mismatch between i_{L1} and i_{L2} is considered attributable to component tolerance.

C. Loss Breakdown

Calculated loss breakdowns are shown in Fig. 15. At the light load of 12 W for both prototypes, MOSFET gate drivers' loss and diode conduction loss were the first and second most dominant loss factors, respectively. Under the heavy load of 36 W, on the other hand, the diode conduction losses as well as collective Joule losses dominated. Contributions of respective Joule losses and switching loss depended significantly on topologies. The Joule loss of switches, for example, was the largest loss contributor in Type 1, whereas that in Type 2 was comparable with the switching loss as well as the Joule loss associated with capacitors.

Detailed calculated loss breakdowns at 36 W are shown in Fig. 16. The loss per diode in Type 2 considerably exceeded that in Type 1 because the diode currents in Type 2 exceeded those in Type 1, as indicated in Tables II and III. However, the collective diode conduction loss in Type 2 was lower than that in Type 1, as shown in Fig. 15, because of the smaller diode count in Type 2.

In Type 1, high voltage rating MOSFETs with relatively high on-resistance were necessary for Q_1 and Q_2. In addition, a large current flowed through Q_2 in Type 1, as indicated in Table II, resulting in considerable Joule loss. In contrast, the collective switching loss in Type 1 was smaller than that in Type 2, as shown in Fig. 15. As can be seen from the current flow directions shown in Fig. 6, Q_3 and Q_4 in Type 1 (as well as Q_5 and Q_6 in Type 2) operate as synchronous switches, causing no switching loss. Therefore, four switches (Q_1–Q_4) in Type 2 caused switching losses, while only two switches (Q_1 and Q_2) in Type 1 contributed, resulting in smaller switching loss in Type 1.

The Joule loss of Q_2 in Type 1 took the significant portion of the total loss, implying that reduction in the on-resistance of Q_2 would be the key to effectively improve its power conversion

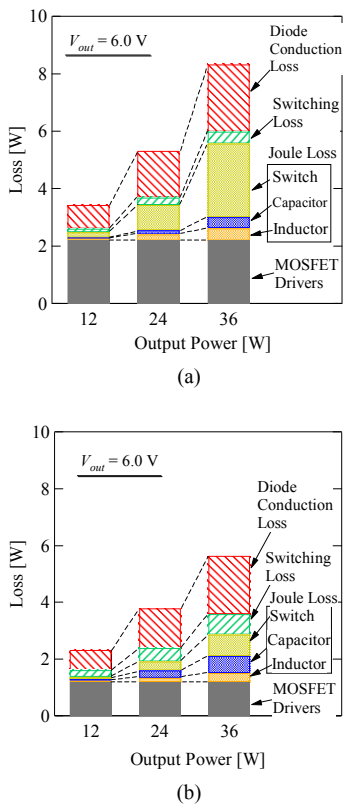

Fig. 15. Calculated loss breakdowns for (a) Type 1 (2s-SCC with 2L-3C SCL cell) and (b) Type 2 (3s-SCC with 1L-2C SCL cell).

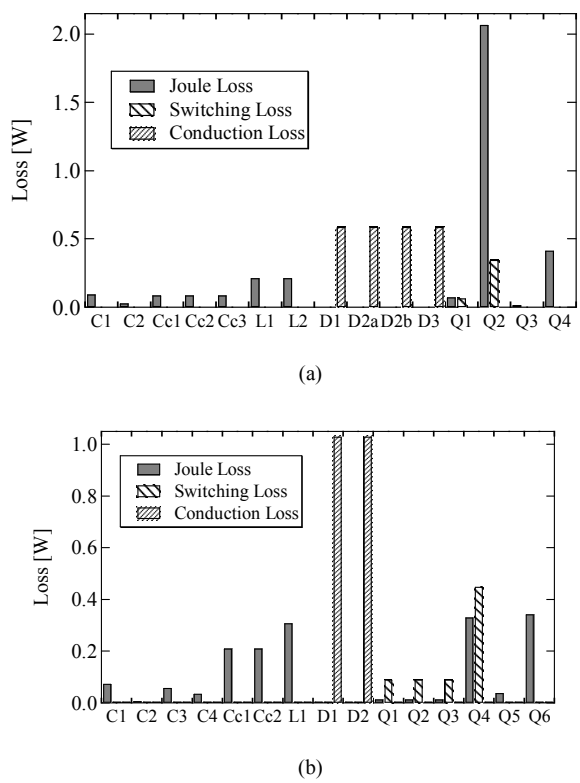

Fig. 16. Detailed loss breakdowns for (a) Type 1 (2s-SCC with 2L-3C SCL cell) and (b) Type 2 (3s-SCC with 1L-2C SCL cell).

TABLE VI
COMPARISON WITH CONVENTIONAL SCCS WITH OUTPUT VOLTAGE REGULATION CAPABILITY

Topology	Control Scheme	Component Count				Efficiency [%]	V_{in} [V]	V_{out} [V]	Conversion Ratio	Power [W]
		C	L	Switch	Diode					
[24]	Resonant	3	1	4	0	82	6	3	0.500	3.35
[31]	PWM	7	1	15	0	81	12	1	0.083	15
[26]	Resonant	3	1	4	0	90	12	12	1.000	22
Proposed (Type I)	PWM	5	2	4	4	80	48	6	0.125	36
Proposed (Type II)	PWM	6	1	6	2	90	48	6	0.125	36
[28]	PWM	4	1	4	0	96	42	14	0.333	140
[27]	Phase Shift	3	1	4	0	99	400	200	0.500	2500

efficiency. Similarly, for Type 2, the switching loss of Q_4 and Joule losses of Q_4 and Q_6 dominated, hence employing a fast-switching low-resistance switch for Q_4 as well as a low-resistance switch for Q_6 would be effective.

VI. COMPARISON WITH VARIOUS SCCS

In this section, the proposed PWM SCCs are compared with previously reported SCCs from various aspects, such as control scheme, component counts, reported power conversion efficiency, and representative voltage conversion ratio. SCCs with output voltage regulation capability are listed in Table IV in the order of power rating. Smoothing capacitors are also included in the capacitor count, although some previous papers do not illustrate input and output smoothing capacitors in their figures for the sake of simplicity.

The reported efficiencies tend to increase with the power rating, and efficiencies of the proposed PWM SCCs are comparable to conventional ones if its power rating is factored in. The efficiency of the proposed Type I PWM SCC is somewhat inferior to conventional ones chiefly due to the large diode conduction loss and gate driver's loss, as revealed in the previous section.

With a given number of switches, the proposed PWM SCCs achieve the greater step-down voltage conversion ratio than do conventional ones. Among the SCCs using four switches, including the proposed Type II SCC and conventional ones [24], [26], [28], [29], the proposed PWM SCC achieves the greatest step-down ratio of 0.125. Although the conventional PWM SCC [31] offers the step-down ratio of 0.083, it requires rather larger number of switches.

VII. EXTENDED TOPOLOGIES

The proposed topologies of PWM SCCs can be further extended using multiple SCL cells and/or different SCC topologies. In the representative topologies discussed in the previous sections, a single PWM cell was used. Replacing multiple energy transfer capacitors with PWM cells can derive extended PWM SCCs with even greater step-down voltage conversion ratios. The topology shown in Fig. 17(a), for example, contains two 1L-2C SCL cells, while its step-down ratio can be yielded similarly to that discussed in Section III, as

$$\frac{V_{out}}{V_{in}} = \frac{d^2}{3d^2 + 3d + 1}. \tag{32}$$

The basic concept of the proposed SCL cell features an energy transfer capacitor in a traditional SCC being replaced with an SCL cell for PWM-controllability as well as high step-down voltage conversion, as discussed in Section II. Therefore, the SCL cell can also be adapted to other SCC topologies, such as series-parallel and Fibonacci SCCs [15], to be a step-down converter. The series-parallel and Fibonacci SCCs with a proposed 1L-2C SCL cell are depicted in Figs. 17(b) and (c), respectively. Their voltage conversion ratio is expressed as

$$\frac{V_{out}}{V_{in}} = \frac{d}{3d + 1}. \tag{33}$$

Thus, the topologies of proposed PWM SCCs can be extended by increasing the number of SCL cells and/or

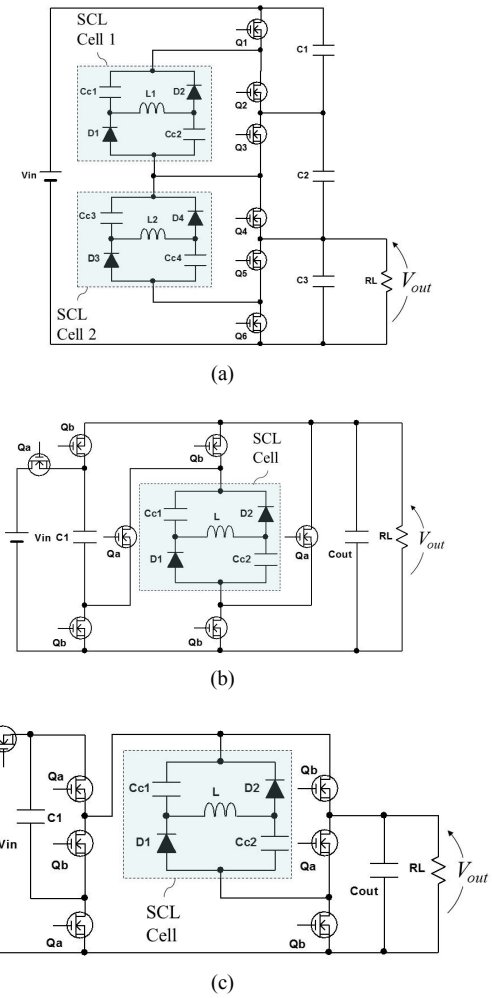

Fig. 17. Extended topologies of PWM SCCs: (a) Ladder SCC with two SCL cells, (b) series-parallel SCC with one SCL cell, (c) Fibonacci SCC with one SCL cell.

employing other SCC topologies. However, as mentioned in Section III-B, a proper topology should be chosen considering the relevant applications and requirement.

VIII. Conclusions

PWM SCCs with adjustable high step-down voltage conversion have been proposed in this paper. The proposed PWM SCCs can be derived based on traditional SCCs by replacing an energy transfer capacitor with an SCL cell that comprises inductors, capacitors, and diodes to realize the PWM-controllability.

The structures of the SCC and SCL cell were generalized, and two representative ladder-SCC-based topologies using different SCL cells were taken as examples for the operational analysis. The voltage step-down ratios of the proposed PWM SCCs are not only PWM-controllable but also adjustable with the structures of both SCCs and SCL cells, allowing flexible design using two design freedoms—structures of SCCs and SCL cells. The relative charge and current flowing through the respective components in the proposed PWM SCCs were mathematically determined based on the charge vector analysis and verified by simulation.

Prototypes of both representative topologies were built, and their measured power conversion efficiencies were compared with calculated ones. The experimental results proved that the proposed PWM SCCs could operate with moderate duty cycles even for high step-down voltage conversion. Measured and calculated efficiencies matched very well, and the loss breakdown analysis revealed that diode conduction losses dominated for both prototypes, while contributions of switching and Joule losses depended significantly on topologies.

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